

[54] SIGNAL PROCESSING DEVICE FOR  
ANALOGUE TO DIGITAL CONVERSION[75] Inventors: Teruki Sugiura, Yamatokooryama;  
Yoshiki Nishioka, Tenri; Noriaki  
Sakamoto, Souraku; Aisaku Taguchi,  
Tenri, all of Japan[73] Assignee: Sharp Kabushiki Kaisha, Osaka,  
Japan

[21] Appl. No.: 399,961

[22] Filed: Aug. 29, 1989

## [30] Foreign Application Priority Data

Sep. 2, 1988 [JP] Japan ..... 63-220711

[51] Int. Cl.<sup>5</sup> ..... H03M 1/00[52] U.S. Cl. .... 341/200; 341/123;  
341/131; 341/139; 341/156[58] Field of Search ..... 341/131, 139, 156, 158,  
341/161, 123, 162, 200

## [56] References Cited

## U.S. PATENT DOCUMENTS

3,729,732	4/1973	Yano	341/162 X
3,855,589	12/1974	Solender	341/158 X
4,198,677	4/1980	Brunner et al.	341/120 X
4,336,525	6/1982	Chapple, III	341/162

4,875,045 10/1989 Lynch et al. .... 341/139

## FOREIGN PATENT DOCUMENTS

59-86328 5/1984 Japan .

61-186025 8/1986 Japan .

61-186026 8/1986 Japan .

Primary Examiner—William M. Shoop, Jr.

Assistant Examiner—Randy Gibson

Attorney, Agent, or Firm—Merchant, Gould, Smith,  
Edell, Welter & Schmidt

## [57] ABSTRACT

A signal processing device comprises a comparator, a first reference signal generating unit, a second reference signal generating unit and reference signal controller and switch which is switched when the data head data of the input signal is detected by the controller. In the case when the content of the input signal is a clock producing data, the reference signal generated in a rapid process of the first reference signal generating unit is entered in the comparator, and in the case when the content of the input signal is a reproduction data, the reference signal generated in a slow process of the second reference signal generating unit is entered in the comparator so as to be compared with the input signal.

2 Claims, 4 Drawing Sheets

